What is claimed is:

1. A sense amplifier, comprising:

a pair of cross-coupled inverters, wherein each inverter includes:

a transistor of a first conductivity type;

a pair of transistors of a second conductivity type coupled at a drain region and coupled at a source region, and wherein the drain region for the pair of transistors is coupled to a drain region of the transistor of the first conductivity type;

a pair of input transmission lines, wherein each one of the pair of input transmission lines is coupled to a gate of a first one of the pair of transistors in each inverter; and

a pair of output transmission lines, wherein each one of the pair of output transmission lines is coupled to the drain region of the pair of transistors and the drain region of the transistor of the first conductivity type in each inverter.

2. The sense amplifier of claim 1, wherein the transistor of a first conductivity type is a p-channel metal oxide semiconductor (PMOS) transistor, and wherein the pair of transistors of a second conductivity type are n-channel metal oxide semiconductor (NMOS) transistors.

3. The sense amplifier of claim 1, wherein the drain region for the pair of transistors and the drain region for the transistor of the first conductivity type in one inverter is further coupled to a gate of the transistor of a first conductivity type and to a gate of a second one of the pair of transistors in the other inverter.

4. A sense amplifier, comprising:

a pair of cross-coupled inverters, wherein each inverter includes:

a p-channel metal oxide semiconductor (PMOS) transistor;

and

a pair of n-channel metal oxide semiconductor (NMOS) transistors coupled at a drain region and a source region, and wherein a drain region of the PMOS transistor is coupled to the drain region for the pair of NMOS transistors;

a bit line coupled to each inverter, wherein each bit line couples to a gate for a first one of the pair of NMOS transistors in each inverter; and

a pair of output transmission lines, wherein each one of the pair of output transmission lines is coupled to the drain region for the PMOS and the NMOS transistors.

5. The sense amplifier of claim 4, wherein the drain region for the PMOS and the NMOS transistors in one of the cross-coupled inverters is further coupled to a gate of the PMOS transistor and to a gate of a second one of the pair of NMOS transistors in the other one of the cross-coupled inverters.

6. The sense amplifier of claim 4, wherein the bit line capacitances are removed from the pair of output transmission lines.

7. The sense amplifier of claim 6, wherein each bit line is coupled to a number of memory cells in an array of memory cells.

8. The sense amplifier of claim 4, wherein the sense amplifier is coupled to a power supply voltage of less than 1.0 Volts.

9. The sense amplifier of claim 8, wherein the sense amplifier is able to output a full output sense voltage in less than 10 nanoseconds (ns).

10. A latch circuit, comprising:

a pair of cross-coupled amplifiers, wherein each amplifier includes:

a first transistor of a first conductivity type;

a second transistor and a third transistor of a second conductivity type, wherein the second and third transistors are coupled at a drain region and are coupled at a source region, and wherein the drain region for the second and third transistors are coupled to a drain region of the first transistor;

a pair of input transmission lines, wherein each one of the pair of input transmission lines is coupled to a gate of the second transistor in each amplifier; and

a pair of output transmission lines, wherein each one of the pair of output transmission lines is coupled to the drain region of the first transistor and to the drain region of the second and the third transistors.

11. The latch circuit of claim 10, wherein the first transistor includes a p-channel metal oxide semiconductor (PMOS) transistor, and wherein the second and the third transistors include n-channel metal oxide semiconductor (NMOS) transistors.

12. The latch circuit of claim 11, wherein the drain region for the PMOS and the NMOS transistors in one of the cross-coupled amplifiers is further coupled to a gate of the PMOS transistor and to a gate of a third transistor in the other one of the cross-coupled amplifiers.

13. The latch circuit of claim 10, wherein the pair of input transmission lines are bit lines and wherein the bit line capacitances are removed from the pair of output transmission lines.

14. The latch circuit of claim 13, wherein each bit line is coupled to a number of memory cells in an array of memory cells.

15. The latch circuit of claim 10, wherein the latch circuit is coupled to a power supply voltage of less than 1.0 Volts.

16. The latch circuit of claim 10, wherein the latch circuit is able to output a full output sense voltage in less than 10 nanoseconds (ns).

17. An amplifier circuit, comprising:

a pair of cross-coupled inverters, wherein each inverter includes:

a transistor of a first conductivity type;

a dual-gated metal-oxide semiconducting field effect transistor (MOSFET) of a second conductivity type, wherein the first transistor of a first conductivity type and the a dual-gated MOSFET are coupled at a drain region;

a pair of input transmission lines, wherein each one of the pair of input transmission lines is coupled to a first gate of the dual-gated MOSFET; and

a pair of output transmission lines, wherein each one of the pair of output transmission lines is coupled to the drain region on each one of the pair of cross-coupled inverters.

18. The amplifier circuit of claim 17, wherein the transistor of a first conductivity type includes a p-channel metal oxide semiconductor (PMOS) transistor, and wherein the a dual-gated MOSFET of a second conductivity type is divided into two separate n-channel metal oxide semiconductor (NMOS) transistors each driven by one of the dual gates.

19. The amplifier circuit of claim 17, wherein the drain region for one of the cross-coupled inverters is further coupled to a gate of the transistor of the first conductivity type and to a second gate of the dual-gated MOSFET in the other one of the cross-coupled inverters.

20. The amplifier circuit of claim 17, wherein the pair of cross-coupled inverters comprise a sense amplifier, and wherein the sense amplifier is included in a memory circuit.

21. The amplifier circuit of claim 20, wherein the sense amplifier is coupled to a power supply voltage of less than 1.0 Volts.

22. The amplifier circuit of claim 21, wherein the sense amplifier is able to output a full output sense voltage in less than 10 nanoseconds (ns).

23. A memory circuit, comprising:

a number of memory arrays;

at lease one sense amplifier, wherein the sense amplifier includes:

a pair of cross-coupled inverters, wherein each inverter includes:

a p-channel metal oxide semiconductor (PMOS) transistor; and

a pair of n-channel metal oxide semiconductor (NMOS) transistors coupled at a drain region and a source region, and wherein a drain region of the PMOS transistor is coupled to the drain region for the pair of NMOS transistors;

a complementary pair of bit lines coupling the at least one sense amplifier to a number of memory cells in the number of memory arrays, and wherein each one of the complementary pair of bit lines couples to a gate of a first one of the pair of NMOS transistors in each inverter; and

a pair of output transmission lines, wherein each one of the pair of output transmission lines is coupled to the drain region of the PMOS transistor and the drain region for the pair of NMOS transistors in each inverter.

24. The memory circuit of claim 23, wherein the memory circuit includes a folded bit line memory circuit.

25. The memory circuit of claim 23, wherein the drain region for the PMOS and the NMOS transistors in one of the cross-coupled inverters is further coupled to a

gate of the PMOS transistor and to a gate of a second one of the pair of NMOS transistors in the other one of the cross-coupled inverters.

26. The memory circuit of claim 23, wherein the at least one sense amplifier is coupled to a power supply voltage of less than 1.0 Volts.

27. The memory circuit of claim 23, wherein the at least one sense amplifier is able to output a full output sense voltage in less than 10 nanoseconds (ns).

28. The memory circuit of claim 23, wherein the memory circuit further includes a number of equilibration and a number of isolation transistors coupled to the complementary pair of bit lines.

29. An electronic system, comprising:

a processor;

a memory device; and

a bus coupling the processor and the memory device, the memory device further including a sense amplifier, comprising:

a pair of cross-coupled inverters, wherein each inverter includes:

a p-channel metal oxide semiconductor (PMOS) transistor; and

a pair of n-channel metal oxide semiconductor (NMOS) transistors coupled at a drain region and a source region, and wherein a drain region of the PMOS transistor is coupled to the drain region for the pair of NMOS transistors;

a complementary pair of bit lines coupling the at least one sense amplifier to a number of memory cells in a memory cell array, and wherein each one of the complementary pair of bit lines couples to a

gate of a first one of the pair of NMOS transistors in each inverter; and

a pair of output transmission lines, wherein each one of the pair of output transmission lines is coupled to the drain region of the PMOS transistor and the drain region for the pair of NMOS transistors in each inverter.

30. The electronic system of claim 29, wherein the sense amplifier is coupled to a power supply voltage of less than 1.0 Volt.

31. The electronic system of claim 29, wherein the sense amplifier is able to output a full output sense voltage in less than 10 nanoseconds (ns).

32. An integrated circuit, comprising:

a processor;

a memory operatively coupled to the processor; and

wherein the processor and memory are formed on the same semiconductor substrate and the integrated circuit includes at least one sense amplifier, comprising:

a pair of cross-coupled inverters, wherein each inverter includes:

a transistor of a first conductivity type;

a pair of transistors of a second conductivity type coupled at a drain region and coupled at a source region, and wherein the drain region for the pair of transistors is coupled to a drain region of the transistor of the first conductivity type;

a pair of bit lines, wherein each one of the pair of bit lines is coupled to a gate of a first one of the pair of transistors in each inverter; and

a pair of output transmission lines, wherein each one of the pair of output transmission lines is coupled to the drain region of the pair of transistors and the drain region of the transistor of the first conductivity type in each inverter.

33. A method for forming a current sense amplifier, comprising:

cross coupling a pair of inverters, wherein each inverter includes:

a transistor of a first conductivity type;

a pair of transistors of a second conductivity type coupled at a drain region and coupled at a source region, and wherein the drain region for the pair of transistors is coupled to a drain region of the transistor of the first conductivity type; and

wherein cross coupling the pair of inverters includes coupling the drain region for the transistor of the first conductivity type and the drain region for the pair of transistors in one inverter to a gate of the transistor of a first conductivity type and to a gate of a first one of the pair of transistors in the other inverter.

34. The method of claim 33, wherein cross coupling the pair of inverters includes forming the first transistor of the first conductivity type as a p-channel metal oxide semiconductor (PMOS) transistor, and forming the pair of transistors of a second conductivity type as n-channel metal oxide semiconductor (NMOS) transistors.

35. The method of claim 33, wherein the method further includes coupling a bit line to a gate of a second one of the pair of transistors in each inverter.

36. The method of claim 33, wherein the method further includes coupling an output transmission line to the drain region for the pair of transistors and the drain region of the transistor of the first conductivity type in each inverter.

37. A method for forming a sense amplifier, comprising:

forming and cross coupling a pair of inverters, wherein forming and cross coupling each inverter includes:

forming a first transistor of a first conductivity type;

forming a second transistor and a third transistor of a second conductivity type, wherein forming the second and the third transistors includes coupling a drain region and a source region for the second and third transistors, and coupling the drain region for the second and third transistors to a drain region of the first transistor;

coupling a bit line to a gate of the second transistor in each inverter; and

coupling an output transmission line to the drain region of the first transistor and to the drain region of the second and the third transistors in each inverter.

38. The method of claim 37, wherein forming the first transistor of a first conductivity type includes forming a p-channel metal oxide semiconductor (PMOS) transistor, and wherein forming the second and third transistors of a second conductivity type includes forming n-channel metal oxide semiconductor (NMOS) transistors.

39. The method of claim 37, wherein cross coupling the pair of inverters includes coupling the drain region for second and third transistors and the drain region for the first transistor of the first conductivity type in one inverter to a gate of the first transistor of a first conductivity type and to a gate of a third transistor in the other inverter.

40. A method for operating a sense amplifier, comprising:

equilibrating a first and second bit line, wherein the first bit line is coupled to a gate of a first NMOS transistor in a first inverter in the sense amplifier and the second bit lines is coupled to a gate of a first NMOS transistor in a second inverter in the sense amplifier;

discharging a memory cell onto the first bit line, wherein discharging a memory cell onto the first bit line drives a signal from a drain region for the first inverter to a gate of a PMOS transistor and to a gate of a second NMOS transistor in the second inverter; and

providing a feedback from a drain region for the second inverter to a gate of a PMOS transistor and a gate of a second NMOS transistor in the first inverter.

41. The method of claim 40, wherein operating the sense amplifier includes operating the sense amplifier with a power supply voltage of less that 1.0 Volts.

42. The method of claim 40, wherein operating the sense amplifier includes latching an output sense signal in less than 10 nanoseconds (ns).

43. The method of claim 40, wherein the method further includes removing the bit line capacitance from a pair of output nodes of the sense amplifier.

44. A method for operating a sense amplifier, comprising:

providing a first bit line signal to a gate of a first NMOS transistor coupled at a drain region and a source region to a second NMOS transistor in a first inverter of the sense amplifier;

providing a second bit line signal to a gate of a first NMOS transistor coupled at a drain region and a source region to a second NMOS transistor in a second inverter of the sense amplifier; and

wherein providing the first and the second bit line signals to the gates of the first and second NMOS transistors isolates the bit line capacitances from a first and second output node on the sense amplifier.

45. A method for operating a sense amplifier, comprising:

providing an input signal from a bit line to a gate of a first transistor in a first inverter of the sense amplifier; and

wherein providing the input signal to the gate of the first transistor isolates the bit line capacitance from an output node on the sense amplifier.